Rejection of Claims 1-33 Under 35 U.S.C.103(a) As Being Unpatentable Over Patapoutian In View of Fredrickson et al. ("Fredrickson")

Claims 1, 10, 20 and 27

Claims 1, 10, 20 and 27 each recite either a palindromic first group of consecutive bits or palindromic first code symbol that represents a logic level.

For example, referring to paragraph 25 and FIG. 5 of the present application, a first group/code symbol has consecutive bits "0000" representing a logic level "0" and a second group/code symbol has consecutive bits "0011" representing a logic level "1". The first group/code symbol "0000" reads the same backward or forward and is thus palindromic.

As acknowledged by the Examiner, Patapoutian fails to teach or suggest palindromic groups/code symbols. As cited by the Examiner, Fredrickson does show a code word, a portion of which ("0000") is palindromic. However, Fredrickson fails in any manner to teach or suggest that this palindromic portion represents a logic level. That is, there's no indication that this palindromic portion, itself, represents a particular logic level. As such, Patapoutian and Fredrickson, either taken each alone or in combination, fail to teach or suggest a palindromic first group of consecutive bits or palindromic first code symbol that represents a logic level.

Claims 2-3, 21-23 and 28-31

Claims 2-3, 21-23 and 28-31 are patentable by virtue of their respective dependencies from claims 1, 10, 20 and 27.

Claims 4, 8, 11, 14, 16 and 24

Claim 4 recites a group of consecutive bits each having a first logic level, the group representing a second logic level. Claims 8 and 24 each recite a first group of four consecutive bits each having a first logic level, the group representing a second (claim 8) or third (claim 24) logic level. Claims 11, 14 and 16 each recite a group of

consecutive bits each having a first logic level, the group representing the first logic level.

For example, referring to paragraph 25 and FIG. 5 of the present application, a code symbol has consecutive bits "0000" representing a servo logic level "0". That is, a servo bit having a logic level "0" is coded as four consecutive logic "0" levels.

Patapoutian, on the other hand, at, *e.g.*, col. 3, Lines 55-58, codes a binary one information value (logic level "1") into a symbol consisting of four consecutive bits "--++" and a binary zero information value (logic level "0") into a symbol consisting of four consecutive bits "++--". As can thus be observed, unlike the claimed group of consecutive bits each having only a first logic level, Patapoutian's groups of consecutive bits each include two different logic levels ("+" and "-"). In other words, to read on the referenced claims, at least one of Patapoutian's groups would have to consist of either "----" or "++++".

Moreover, Fredrickson fails to supply the teachings missing from Patapoutian, namely a group of consecutive bits each having a first logic level, the group itself representing a logic level.

Claims 5-7, 9, 12, 13, 15, 17-19, 25 and 26

Claims 5-7, 9, 12, 13, 15, 17-19, 25 and 26 are patentable by virtue of their respective dependencies from Claims 4, 8, 11, 14, 16 and 24.

Claim 32

Claim 32 recites a sequence comprising a first group of consecutive bits, the first group having first and second portions and representing a first logic level, the first portion preceding the second portion, the bits in the first portion each having a second logic level and the bits in the second portion each having a third logic level, and a second group of consecutive bits, the second group having first and second portions and representing a fourth logic level, the first portion of the second group preceding the second portion of the second group, the bits in the first portion of the second group each

having the second logic level and the bits in the second portion each having a fifth logic level different from the third logic level.

For example, referring to paragraph 25 and FIG. 5 of the present application, a first group has consecutive bits "0000" representing a first logic level "0" and a second group has consecutive bits "0011" representing a fourth logic level "1". The first group has a first portion "00" preceding a second portion "00." The bits in the first-group first portion each have a second logic level "0" and the bits in the first-group second portion each have a third logic level "0." The second group has a first portion "00" preceding a second portion "11." The bits in the second-group first portion each have the second logic level "0" and the bits in the second-group second portion each have a fifth logic level "1" different from the third logic level "0."

Patapoutian, on the other hand, at, *e.g.*, col. 3, Lines 55-58, codes a binary one information value (logic level "1") into a symbol consisting of four consecutive bits "--++" and a binary zero information value (logic level "0") into a symbol consisting of four consecutive bits "++--". Each of these groups can be divided into portions "--" and "++." As can thus be observed, in any given sequence of Patapoutian's bit groups, it will never be the case that a first-group first portion preceding a first-group second portion will have the same logic level as a second-group first portion preceding a second-group second portion having a logic level different from that of the first-group second portion. In other words, to read on claim 32, Patapoutian's bit groups would have to consist of, for example, "--++" and "----". One of his bit groups must either consist of "----" or "++++" in order to read on claim 32 or claim 33.

Moreover, Fredrickson fails to supply the teachings missing from Patapoutian, namely a sequence, each group of which represents a logic level and has portions arranged in the manner claimed and discussed above.

Claim 33

Claim 33 is patentable for reasons similar to those discussed above in connection with claim 32.

CONCLUSION

In view of the foregoing, all claims are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes that a telephone conference would expedite prosecution of this application, please telephone the undersigned at 425.455.5575. If the Examiner does not agree that all claims are in condition for allowance, the Examiner is respectfully requested to telephone the undersigned prior to issuing an advisory action in this case.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

Respectfully submitted,

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